LINEAR TECHNOLOGY

DESIGN NOTES

Pass HDMI Compliance Tests with Ease – Design Note 394

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Introduction

The high definition multimedia interface (HDMI) is fast becoming the de facto standard for passing digital audio and video data in home entertainment systems. This standard includes an I²C type bus called a display data channel (DDC) that is used to pass extended digital interface data (EDID) from the sink device (such as a digital TV) to the source device (such as a digital A/V receiver). EDID includes vital information on the digital data formats that the sink device can accept. The HDMI specification requires that devices have less than 50pF of input capacitance on their DDC bus lines, which can be very difficult to meet. The LTC®4300A's capacitance buffering feature allows devices to pass the HDMI DDC input capacitance compliance test with ease.

LTC4300A-1 Bus Buffer

The LTC4300A-1 is a 2-wire bus buffer that includes capacitance buffering between input and output, an enable pin for input-to-output connection control through hardware and rise time accelerators to provide for swift bus transitions through the bus logic thresholds. Due to the sub-10pF input capacitance of the LTC4300A-1, the capacitance buffering right at the HDMI connector interface allows the component to easily pass the DDC input capacitance test limit of 50pF even if the internal capacitance of the channel is substantially higher. The HDMI cable connector must see the OUT side of the LTC4300A-1 for the input capacitance compliance testing to be accurate.

In HDMI, the sink pulls the hot plug detect (HPD) signal high to tell the source that it is ready to accept commands through the DDC. This signal can be controlled by the READY pin of the LTC4300A-1 to prevent the possibility of erroneous attempts by the source to contact the sink before the sink is ready to return EDID. The READY pin only goes high after 5V is applied and the LTC4300A-1 ENABLE pin is pulled high by the HDMI receiver IC, a controller in the sink, or the 5V line itself.

The rise time accelerators in the LTC4300A-1 compress transition times on rising signal edges, minimizing the chance of interrupted data transfer due to noise and allowing the DDC to meet I²C timing requirements. That is, HDMI specification allows for 800pF of load; enough that the DDC cannot be guaranteed to meet the required 100kHz I²C 1µs rise time specification with the allowed DDC pullup resistance values. Rise time accelerators allow this timing requirement to be met even with capacitances well above 800pF.

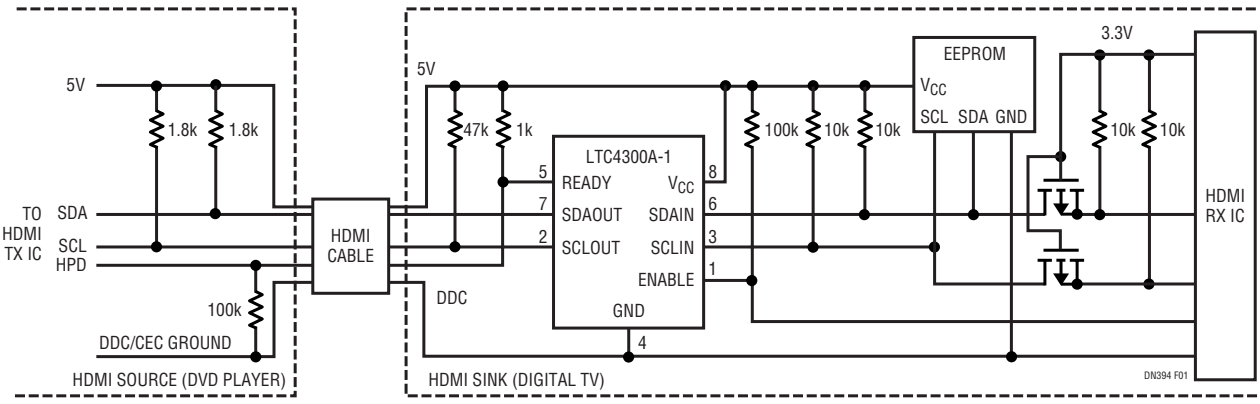

Figure 1. LTC4300A-1 in HDMI Capacitance Buffering Application

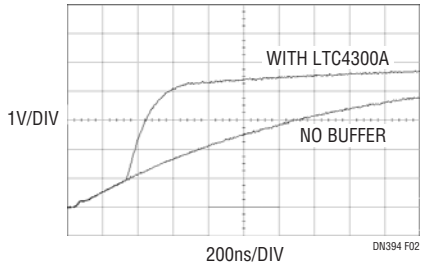

Figure 2. The LTC4300A Provides Capacitance Buffering for the DDC while Improving Bus Timing

If the 5V supply for the DDC is changed to 3.3V in future versions of the HDMI specification, the LTC4300A-1 can remain in the design as is, for it can work with supply voltages from 2.7V to 5.5V. The LTC4300A-1 will transparently support new and legacy equipment in the case of an HDMI specification change.

Figure 2 shows how the LTC4300A-1 provides capacitance buffering at the cable interface while improving the rise time of the heavily loaded 5V bus (750pF in this example). Without the LTC4300A-1, the signal is failing the I^2C 1µs rise time specification (measured between $0.3V_{CC}$ and $0.7V_{CC}$). In the DDC capacitance test, only the capacitance of the connector, the traces to the LTC4300A-1 and the less than 10pF input capacitance of the LTC4300A-1 will be measured.

LTC4300A-3 Level Shifting Buffer

The LTC4300A-3 level shifting I^2C buffer is also a good solution for this application. Figure 3 shows the LTC4300A-3 being used for capacitance buffering and 5V to 3.3V level shifting. In this application, the EEPROM is powered by a backup 3.3V supply that is available when the component is turned off. The EDID in the EEPROM should be available for reading even when a component's power is off. The level shifting between the 5V and 3.3V bus segments is accomplished by having separate supply pins for the two segments.

Having two supply pins also allows the LTC4300A-3 to provide rising edge acceleration on the 3.3V and 5V bus segments. This is a useful feature for the bus segment that is inside the component, but cable capacitance values of well over the 700pF HDMI spec will be encountered in the up to 30m HDMI cables that are being used for home theaters, so rise time acceleration is a most valuable feature on the cable side bus segment.

Although the applications shown are for HDMI receive channels, the LTC4300A-1 and LTC4300A-3 can also be used in HDMI transmit channels with equal success.

Conclusion

The LTC4300A-1 and LTC4300A-3 solve the DDC capacitance testing problem in HDMI while also substantially improving the timing performance of the bus and providing a high level of ESD protection.

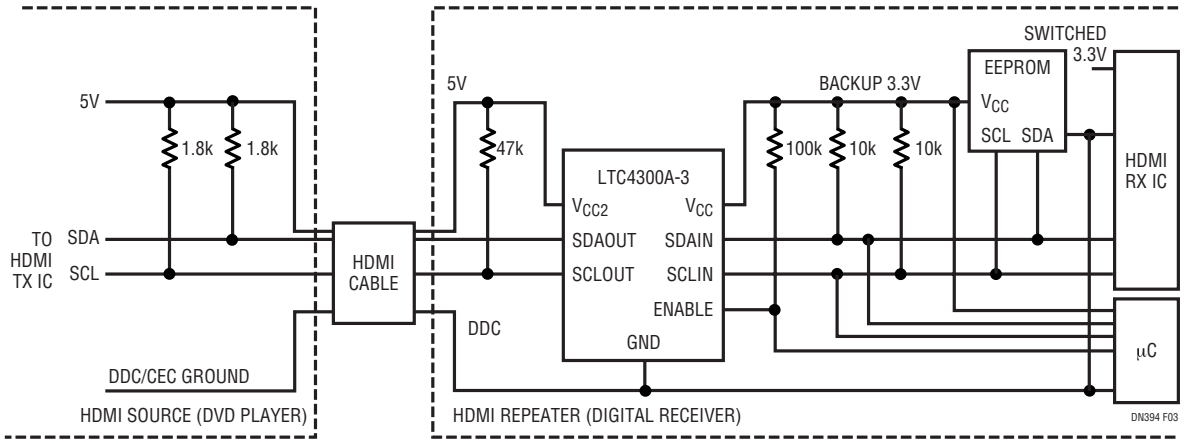

Figure 3. LTC4300A-3 in a Level Shifting and Capacitance Buffering HDMI Application with Backup 3.3V

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